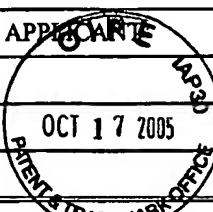




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						M-15302-1P US		10/798,540	
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(Use several sheets if necessary)						Savastiouk et al.			
						Filing Date		Group	
						March 10, 2004		2812	
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
KL	AA	6,322,903	Nov. 2001	Siniaguine et al.					
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	AE								
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	AH								
	AI								
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Foreign Patent Documents									
							Translation		
		Document	Date	Country	Class	Subclass	Yes	No	
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	AL								
	AM								
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)									
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Examiner		<i>[Signature]</i>							
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KL	AA	2002/0048916	25 Apr. 2002	Yanagida			
	AB	6,175,158	16 Jan. 2001	Degani et al.			
	AC	2003/0080437	1 May 2003	Gonzalez et al.			
	AD	6,661,088	9 Dec. 2003	Yoda et al.			
	AE	2002/0036340	28 Mar. 2002	Matsuo et al.			
	AF	2003/0047798	13 Mar. 2003	Halahan			
	AG	2002/0074637	20 Jun. 2002	McFarland			
	AH	2002/0175421	28 Nov. 2002	Kimura			
↓	AI	2003/0116859	26 Jun. 2003	Hashimoto			
KL	AJ	6,322,903	27 Nov. 2001	Siniaguine et al.			

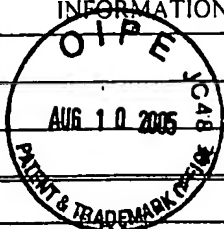
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KL	AK	195 31 158 A1	27 Feb. 1997	DE			X	
KL	AL	08-236579	13 Sept. 1996	JP			X	
KL	AM	0 193 128	3 Sept. 1986	EP			X	

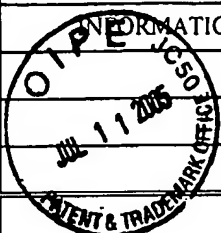
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KL	AN	"Solving Soldering Hierarchy Problems by Metallurgy and Design" IBM Technical Disclosure Bulletin, IBM Corp. New York, US, vol. 33, no. 8, January 1991, pages 298-299, XP000106967, ISSN: 0018-8689

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	AE	2002/0074637	20 Jun. 2002	McFarland				
	AF	2002/0175421	28 Nov. 2002	Kimura				
	AC	2003/0080437	1 May 2003	Gonzalez et al.				
KL	AH	2002/0048916	25 Apr. 2002	Yanagida				
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	AL	Ekstrom; Bjorn "Thin Film Silicon Substrates For Lead Frame Packages" Advancing Microelectronics - May/June 2003, pages 6-7.
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	AQ	Sperling, Ed; Electronic News, 9/17/2003.	
	AR	"Introduction to Printed Wiring Boards" Netpack Education Pool, page 1-18.	
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	AX	Moon, K.W.; Boettinger, W.J.; Kattner, U.R.; Biancaniello, F.S.; Handwerker, C.A. "The Ternary Eutectic of Sn-Ag-Cu Colder Alloys" Metallurgy Division, Materials Science and Engineering Laboratory NIST Gaithersburg, MD 20899 USA.	
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	BA	United States Patent Application No. 10/739,707, entitled "Packaging Substrates For Integrated Circuits and Soldering Methods," Filed on December 17, 2003; Attorney Docket No.: M-15278 US.	
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	BE	Gektin, Vadim; Bar-Cohen, Avram; Witzman, Sorin "Coffin-Mason Based Fatigue Analysis of Underfilled DCAs," 1998 IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A, Volume 21, No. 4, December 1998, pages 577-584.	
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